Listing and/or Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) An apparatus for isolating a noise intolerant device from a source of noise, comprising:

a processor for producing clock and data signals and a control signal; and

a digital bus that couples said clock and data signals to a buffer,

where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

2. (Currently Amended) The apparatus of claim 1, wherein said digital bus is an inter integrated circuit (IIC) bus, and the apparatus further comprises an IIC bus expander for transferring said control signal to said buffer.

3. (Currently Amended) The apparatus of claim 1, wherein the digital bus comprises:

an IIC bus having a clock signal path for transferring clock pulses from said processor to ~~said~~ clock inputs of ~~said~~ an IIC bus expander and said buffer;

a data signal path for transferring data from said processor on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander and said buffer; and

wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device from said IIC bus and said processor.

4. (Previously Presented) The apparatus of claim 3, wherein said noise intolerant device comprises:

a tuner, coupled to said clock and data outputs of said buffer device, having a phase-lock loop for generating frequency variable tones, and a down-converter coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal.

5. (Previously Presented) The apparatus of claim 4, wherein said buffer comprises:

a first OR gate and a second OR gate, each of said first and said second OR gates having a first input coupled to said output of said IIC bus expander;

a second input said first OR gate coupled to a clock signal path of said IIC bus, and a second input of said second OR gate coupled to a data signal path of said IIC bus; and

an output of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop, and an output of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop.

6. (Withdrawn)

7. (Withdrawn)

8. (Withdrawn)

9. (Withdrawn)

10. (Withdrawn)

11. (Withdrawn)